On the Turbo Coded Bits Allocation Mode for the 64-QAM Square Modulation

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***Abstract*—This paper presents a study on turbo coded bit allocation in the modulator symbol for square quadrature amplitude modulation with 64 signal points. The simulations have involved both single binary turbo code of the LTE standard with coding rates 1/3 and 2/3 and double binary turbo code of the DVB-RCS2 with coding rate 2/3. The simulation results show that different investigated allocation methods affect dramatically the performance of bit/frame error rate versus signal to noise ratio of the turbo coded system. Hierarchies in performance of the allocation methods are completely different in regions with water fall versus error floor.**

***Keywords*—AWGN channel, communication systems, mapping, quadrature amplitude modulation, turbo code.**

I. Introduction

QUADRATURE amplitude modulation (QAM) is frequently met in current communication systems. Specific standardized applications use specific variants of QAM. Variants of QAM are used in digital cable television or wireless and cellular technology applications. The 64-QAM is a good compromise between spectral efficiency (6 bit/s/Hz) and performance of bit/frame error rate (B/FER) versus signal to noise ratio (SNR) **[1]**. 64-QAM gives a symbol error rate of 10^{-6} for a SNR of about 19 dB for uncoded system. However, using a turbo code, a BER of 10^{-10} can be obtained at a SNR of 9 dB. The square 64-QAM is the most frequently encountered in applications. For example, in LTE is specified that such modulation techniques with Gray allocation can be used to minimize the BER **[2]**.

A specific property of squares QAM modulations with Gray allocation is that the bits of the symbol modulator are not uniform protected. The same non uniform protection characterizes the square 64-QAM modulation. A question arises in the case of a direct coupling between the turbo encoder and the modulator : "Which bits of the encoded symbol must be better protected by the QAM in order to obtain a better system performance?". Our previous studies have been dedicated to the same question for square 16 and 256-QAM **[3]**, **[4]**, using the double-binary turbo codes (DBTC) of the DVB-RCS standards **[5]**, **[6]**. In the present paper we study the square 64-QAM, turbo coded not only with DBTC but also with the single binary turbo code (SBTC) of the LTE **[2]**.

In this paper we have analyzed three location for the placement of the information and parity bits generated by turbo coding in the symbol modulator. In the first case for both SBTC coding rates, 1/3 and 2/3, the information bit was placed in the best protected position, followed by two parity bits placed in less protected positions. In the second case the information bit is placed on the middle position, so that in the better and less protected positions are placed the parity bits. Finally, in the third case, the information bit appears on the poorly protected position. The results of simulations show a completely different behavior in the performance of B/FER vs SNR of these allocation variants.

The structure of this work is organized as follows. In Section II are presented the turbo encoders used in this paper (single binary - SBTE and double binary - DBTE) in order to identify the bits to be allocated in the symbol modulator. Section III briefly describes the square 64-QAM with the same aim to identify positions from the modulator symbol that will be filled by turbo encoded bits, nominated previously. Section IV is dedicated to presenting allocation alternatives. Section V shows the simulation results and Section VI concludes the paper.

II. The Turbo Encoder

The structure of the turbo encoder and puncturing matrix are the factors that determine the composition of the turbo coded block. This section describes the SBTE specified in **[2]** and the DBTE specified in **[6]**, as well as the puncturing matrices used to derive coding rate 2/3.

A. Single binary turbo encoder

Fig. 1 shows the structure of a SBTE. Input sequence u is encoded directly by the convolutional encoder C1 and via interleaver (π) by the encoder C0. Depending on the required,

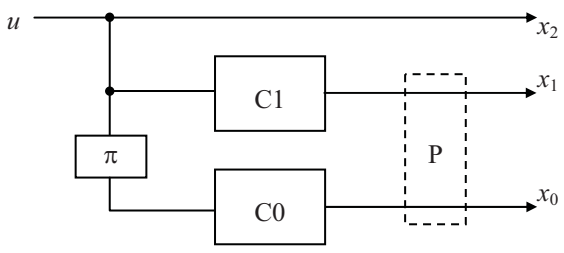

Fig. 1. The scheme of a SBTE.

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