On the Double-Binary Turbo Coded Bits Allocation Mode in the Case of 256-QAM Square Modulation

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Abstract—This paper presents a study concerning the allocation possibilities of the bits generated by the double binary turbo encoder (DBTE) in the modulator symbol, in the case of the quadrature amplitude squared modulation with 256 signal points (256-QAM), in AWGN channel. We compared the bit/frame error rate (B/FER) versus signal to noise ratio (SNR) performances of memory 3 and 4 double-binary turbo codes (DBTC), defined in DVB-RCS and DVB-RCS2 standards. We considered both DBTC common coding rate, ¹/₂, and the coding rate of ³/₄ obtained using puncturing. The simulations results lead to certain conclusions for the selection of the best allocation methods, both in the water fall region and in error floor region.

Keywords—AWGN channel, communication systems, mapping, quadrature amplitude modulation, turbo code.

I. INTRODUCTION

THE 256-QAM modulation offers a high spectral efficiency [1]. However, even if it is used in conjunction with turbo coding, 256-QAM modulation can be used in transmission channels having a very good SNR (see for example [2]). Perhaps this is why 256-QAM modulation is less common in publications that are considering coding modulation. But, while the transmission channels will have an increasing immunity to disturbances, (turbo) coding 256-QAM modulation will become interesting.

In this paper, we presented a study regarding B/FER vs. SNR performances of a communication system incorporating DBTC and 256-QAM square modulation. Because both the DBTE output and the input of 256-QAM modulator are formed by multi-binary symbol sequences, it is possible to design the mapping between the two, in various ways. The performances obtained using these mapping modes between encoding and modulation represents the object of the presented paper. The rest of the paper is structured as follows. In Section 2, we will present the scheme of a DBTE and the structure of the block generated by the DBTE. Section 3 presents the signals diagram for 256-QAM square modulation. We considered a Gray allocation between the octa-binary symbol and the signals points from the diagram. In Section 4, we proposed several mapping ways between the quadri-binary

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Horia Balta is also with Faculty of Electrical Engineering, Electronics and Information Technology, Valahia University of Targoviste, 2 Avenue King Carol I, 130024, Romania. symbol from the DBTC output and the octa-binary symbol from the modulator input. These modes essentially differ, depending on the used coding rate. In the present study, we considered two coding rates: ¹/₂ and ³/₄. The B/FER vs. SNR performances obtained using these mapping modes are presented in section 5. The conclusions drawn from the analysis of the simulation results, obtained by choosing the most efficient mapping ways, are given in Section 6.

II. DOUBLE BINARY TURBO ENCODER

In Fig. 1 the scheme of a DBTE is presented [3]. The scheme has two inputs and four outputs. So, in the absence of puncturing, the (turbo) coding rate is $R_c = 2/4 = 0.50$. The input data block has a matrix structure with the dimension $2 \times N$, where N is the inter-symbol interleaving length, fixed by the interleaving block, π . This block performs double interleaving, intra- and inter-symbol, where the (input) symbol actually means the pair (u_1, u_2) (see [4]). The convolutional encoders C0 and C1, having the coding rate equal to 2/3, generate the parity sequences x_0 and x_1 . Thus, an DBTE output block is a is a binary array (matrix) with the size $4 \times N$, in which each column contains the 4 bits $x_i = (x_3^J, x_2^J, x_1^J, x_0^J)$. The first two are information bits and the last two are parity bits. In order to obtain a coding rate $R_c > 1/2$ we can use the puncturing procedure. Thus, the block P in Fig. 1 erases some of the parity bits following a rule given by the puncturing mask. In order to obtain a coding rate equal to 0.75 we used the following puncturing mask:

$$M_{p} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix},$$
 (1)

where with zeros we have marked the bits to be cleared. In this way, the structure of the turbo encoded block will be:



Fig. 1. The scheme of a DBTE.